High aspect-ratio InGaAs FinFETs with sub-20 nm fin width

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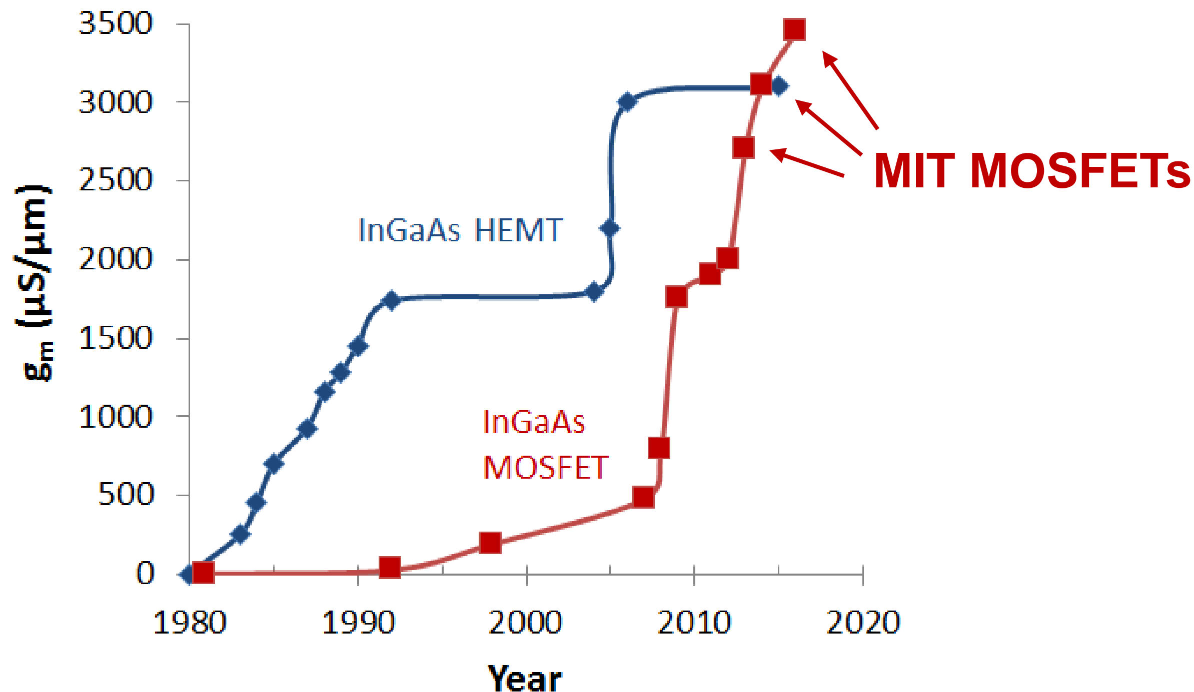
Lam Research

Outline

- Motivation
- Process technology
- Electrical characteristics
- Late news
- Conclusions

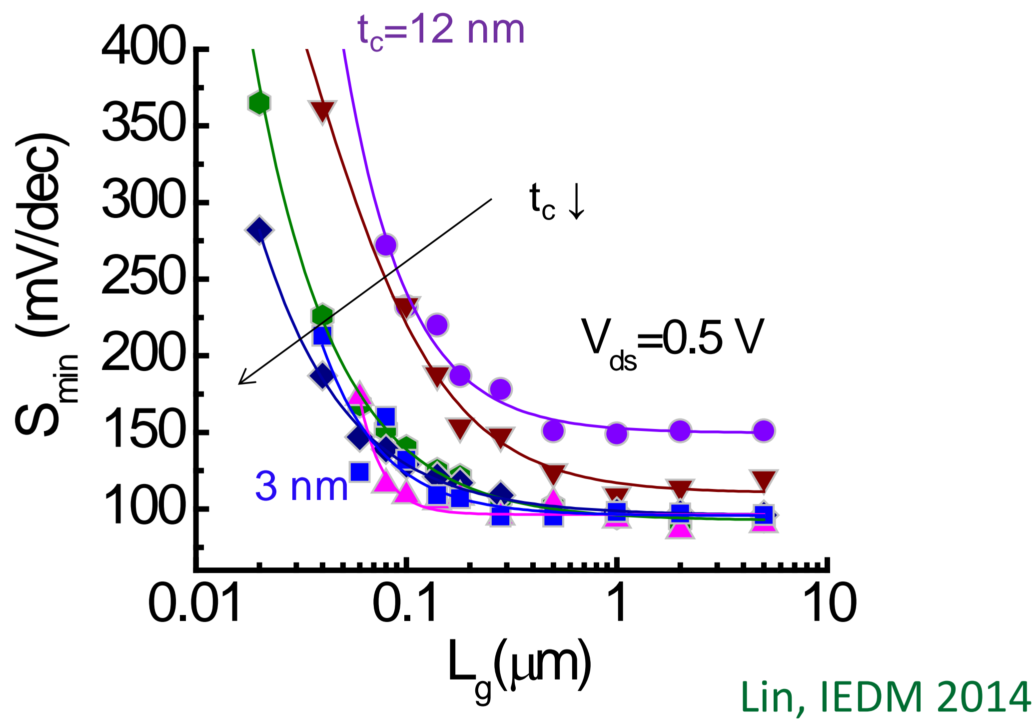
InGaAs planar Quantum-Well MOSFETs



del Alamo, J-EDS 2016

- Superior electron transport properties in InGaAs
- InGaAs planar MOSFET performance exceeds that of High Electron Mobility Transistors (HEMT)

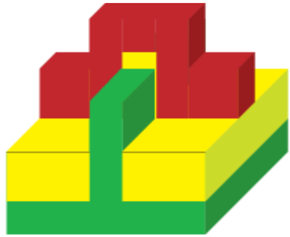
InGaAs planar Quantum-Well MOSFETs - short-channel effects



Lin, IEDM 2014

- Short-channel effects limit scaling to L_g~40 nm
- 3D transistors required for further scaling

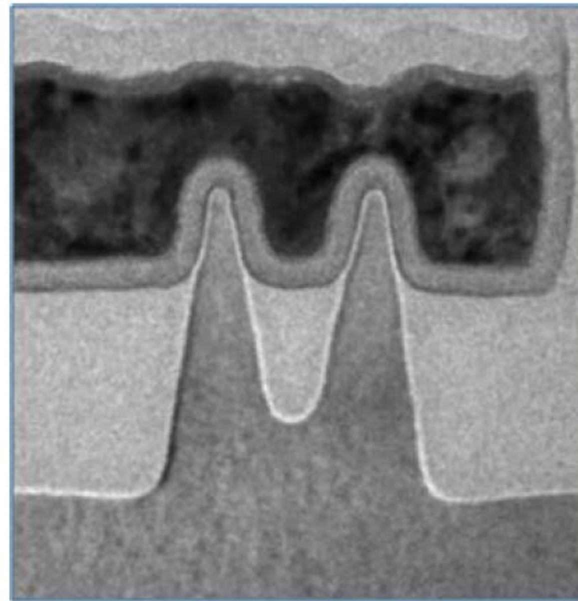
FinFETs



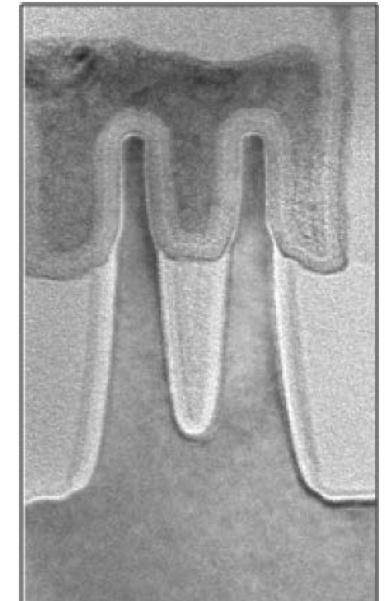
Double-gate MOSFET

Tri-gate MOSFET

Intel Si Trigate MOSFETs



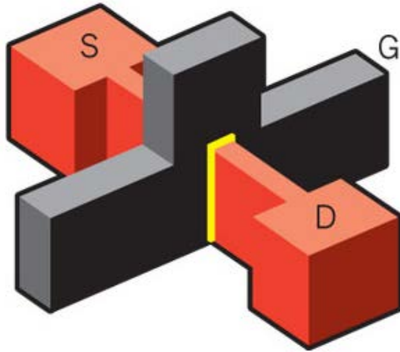
22 nm Process

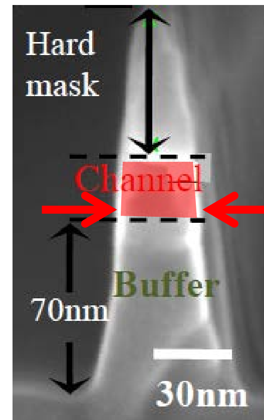


14 nm Process

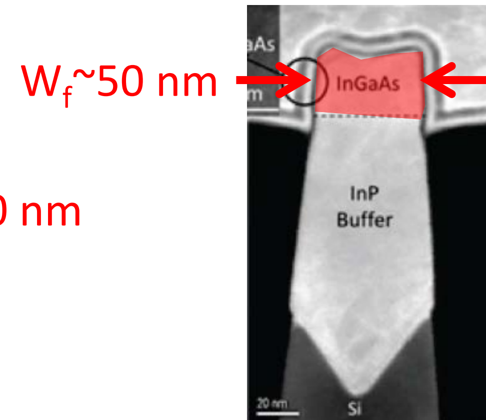
- FinFETs are use in modern state-of-the-art technologies
- Good balance of SCE and high ON current per footprint

InGaAs FinFETs

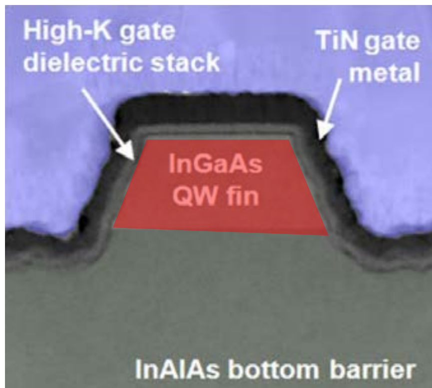




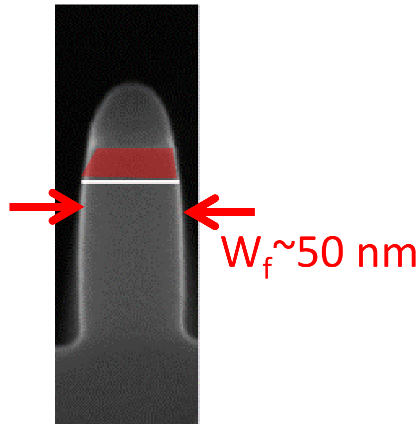
Thathachary, VLSI 2015



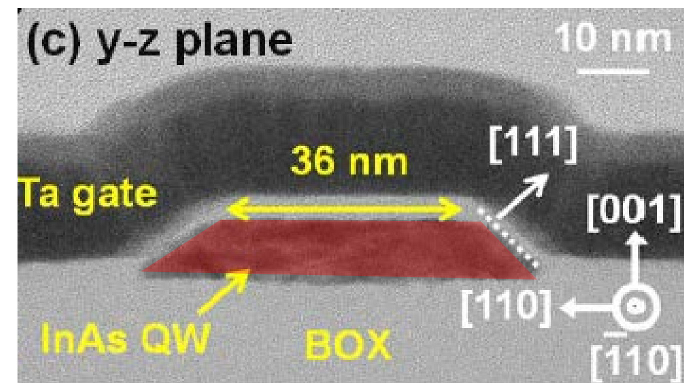
Waldron, VLSI 2014



Radosavljevic ,IEDM 2011



Kim, IEDM 2013

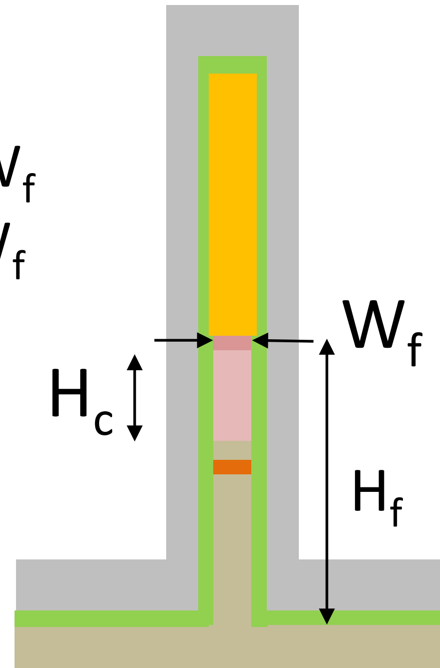


Kim, TED 2014

- Demonstrations to date: $W_f \geq 25$ nm, $AR_c \leq 1$

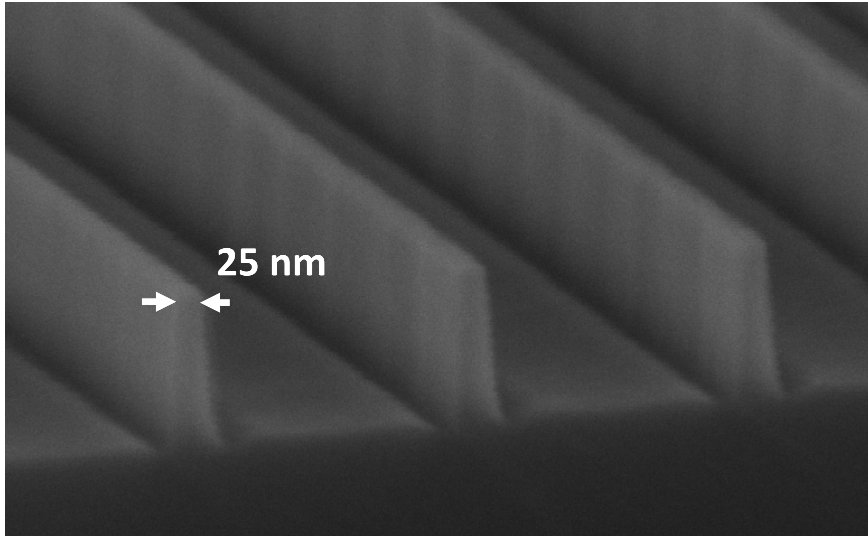
Goal: Sub-20 nm W_f Self-aligned III-V FinFETs

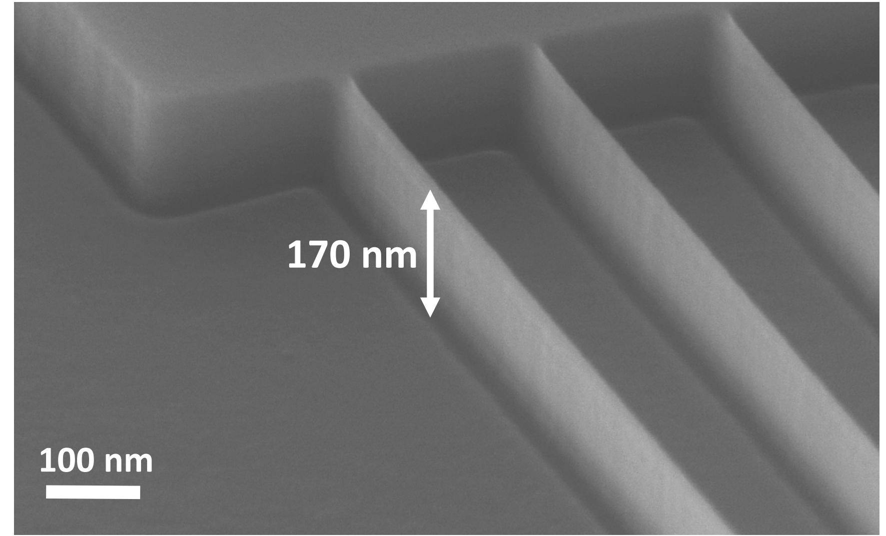
$$AR_c = H_c/W_f$$
$$AR_f = H_f/W_f$$



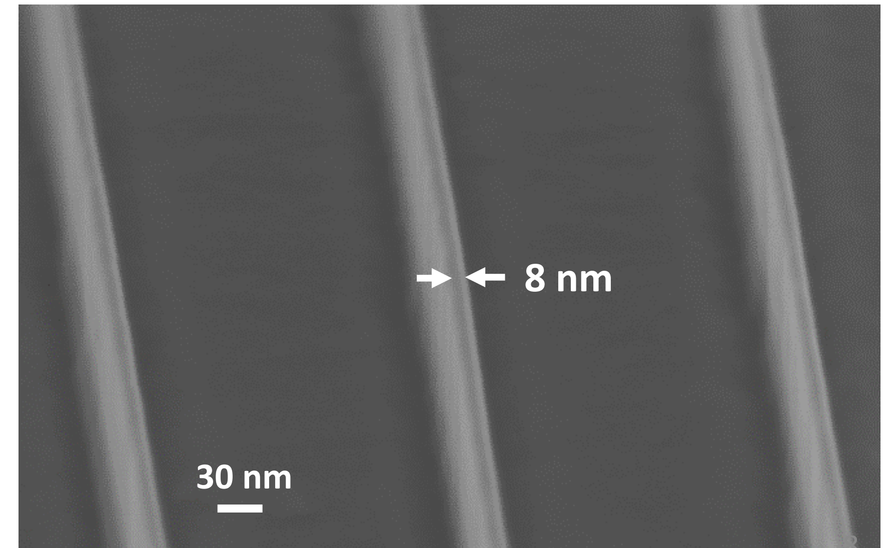
- Deeply scaled fin width, gate length and gate oxide
- High channel to fin width aspect ratio (AR_c)
- Self-aligned contacts
- CMOS-compatible processes and materials in front-end

Fin definition:
Dry etch + Digital etch

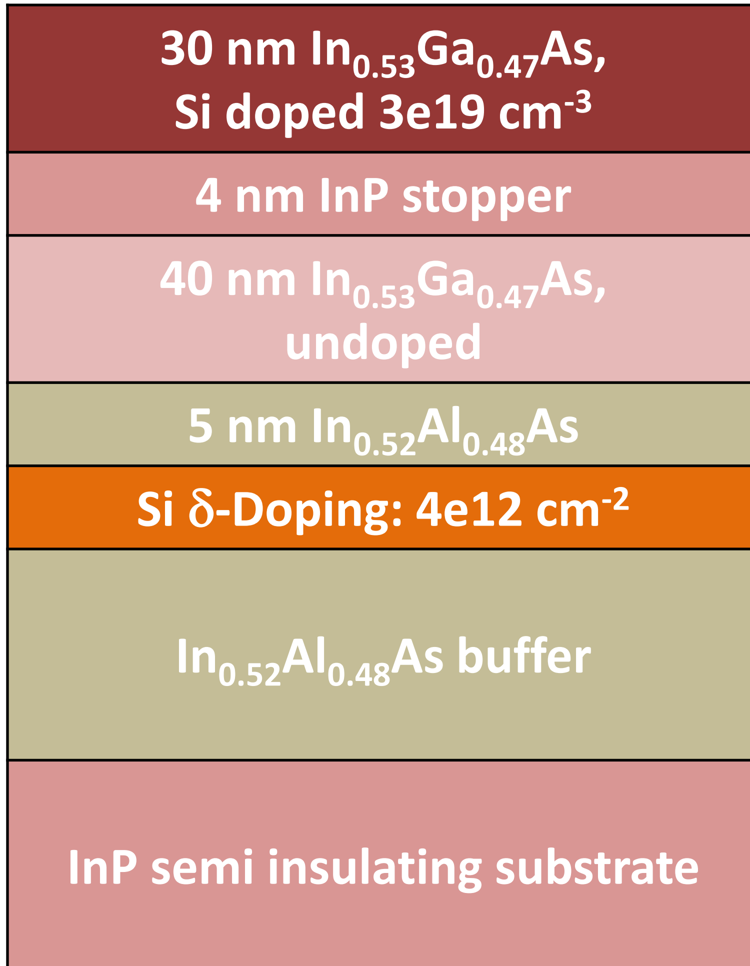




- **$BCl_3/SiCl_4/Ar$ RIE** of InGaAs nanostructures with smooth, vertical sidewalls and high aspect ratio (>10)
- **Digital etch (DE)**: self-limiting O_2 plasma oxidation + H_2SO_4 oxide removal

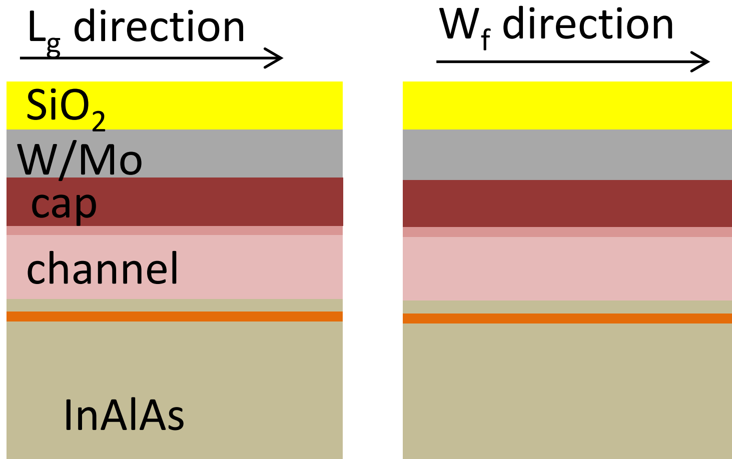


Device fabrication



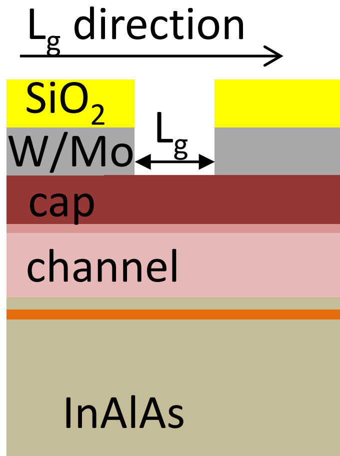
- Highly doped cap
- 40 nm thick channel layer
- Delta doping underneath

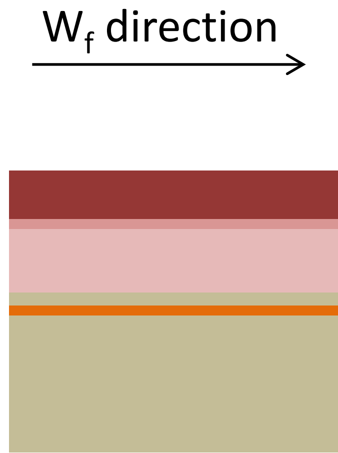
Device fabrication

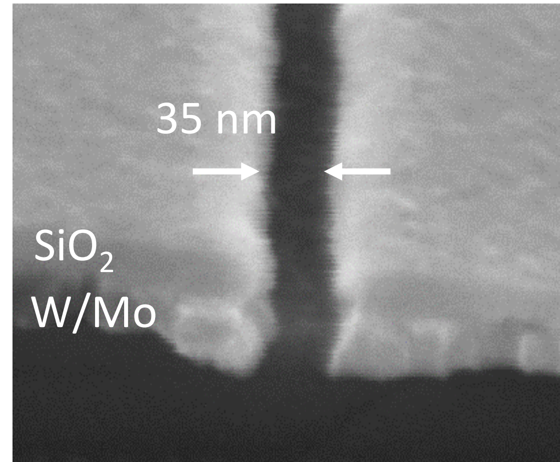


- Sputtered W/Mo contact
- CVD SiO_2 hard mask

Device fabrication

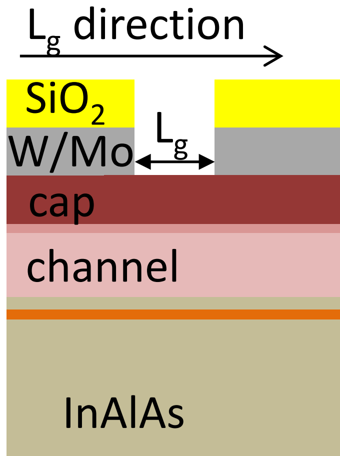


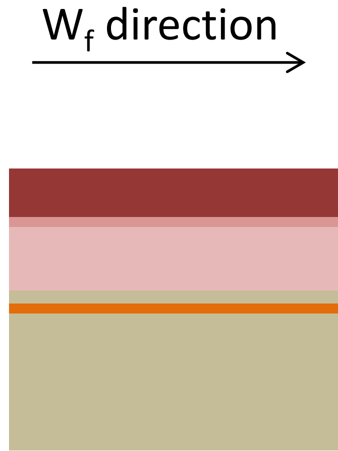


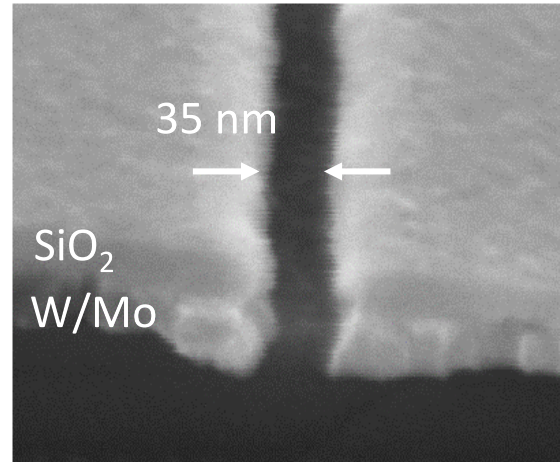


- Sputtered W/Mo contact
- CVD SiO_2 hard mask
- Gate lithography
- Gate recess (Dry): SiO_2/W/Mo
- Active area definition

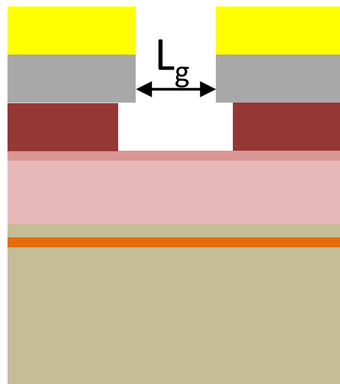
Device fabrication

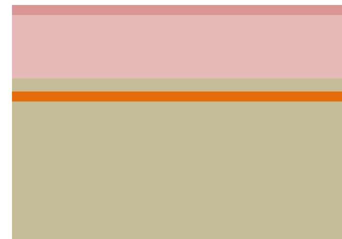


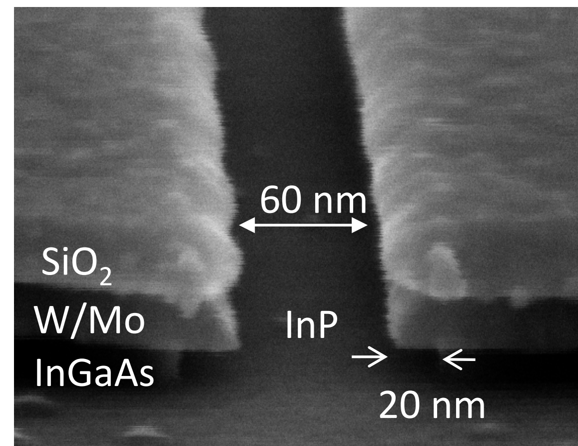




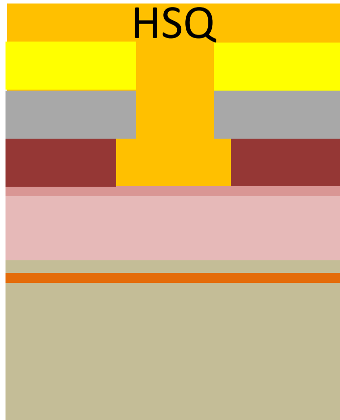
- Sputtered W/Mo contact
- CVD SiO_2 hard mask
- Gate lithography
- Gate recess (Dry): SiO_2/W/Mo
- Active area definition
- Gate recess (Wet): Cap etch

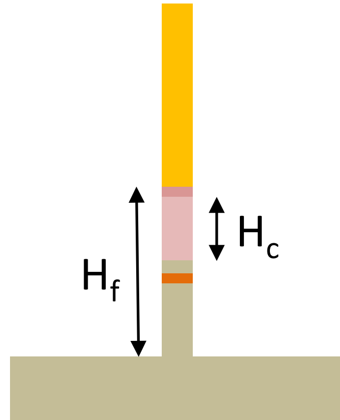


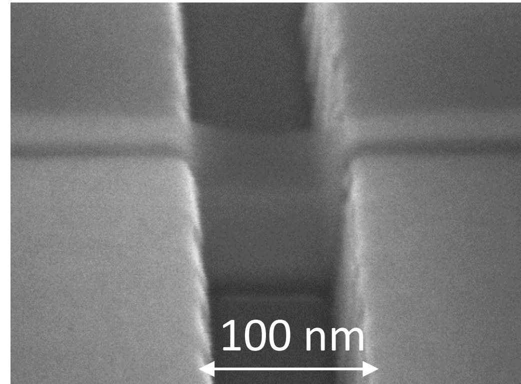


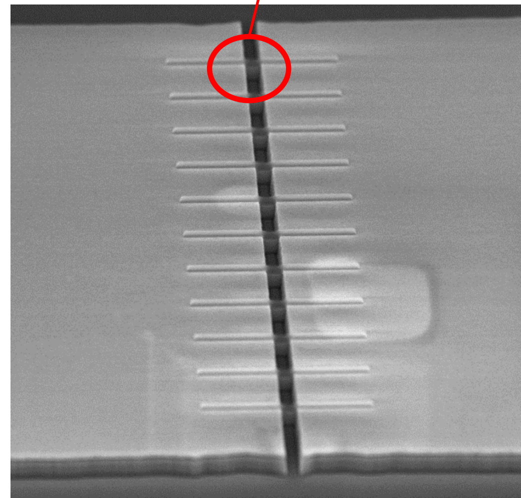


Device fabrication



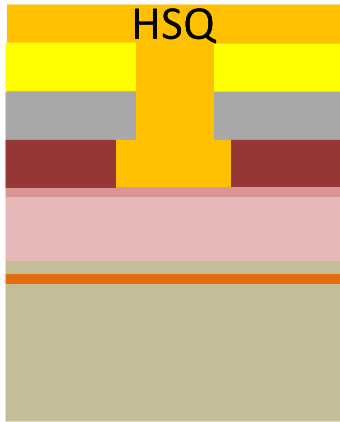


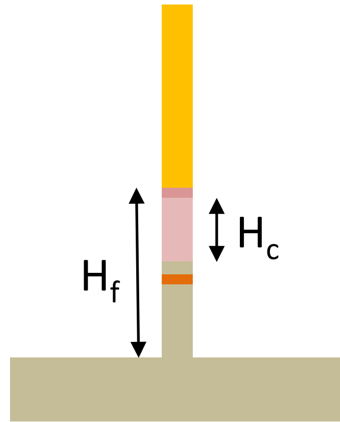


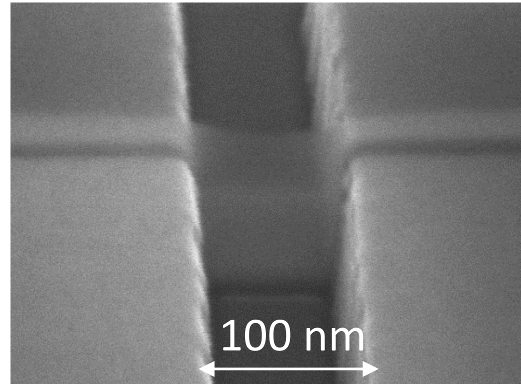


- Sputtered Mo contact
- CVD SiO_2 hard mask
- Gate lithography
- Gate recess (Dry): SiO_2/W/Mo
- Active area definition
- Gate recess (Wet): Cap etch
- Fin Lithography
- Fin etch

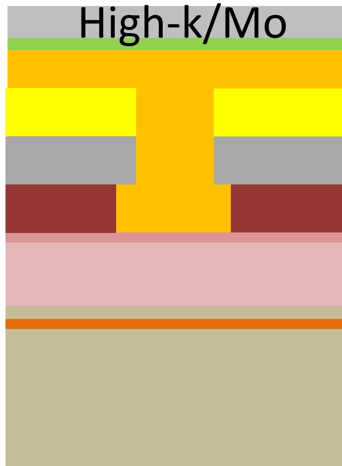
Device fabrication

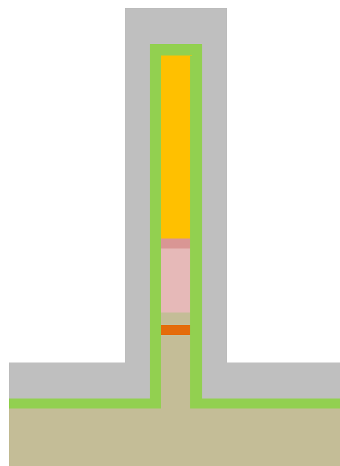


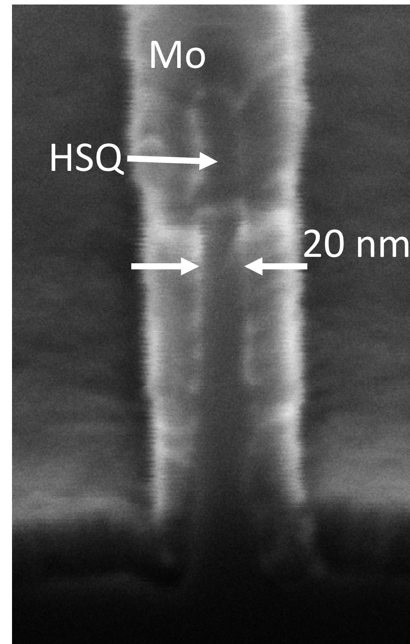




- Sputtered W/Mo contact
- CVD SiO_2 hard mask
- Gate lithography
- Gate recess (Dry): SiO_2/W/Mo
- Active area definition
- Gate recess (Wet): Cap etch
- Fin lithography
- Fin etch
- Digital etching
- ALD gate dielectric deposition
- Mo gate sputtering

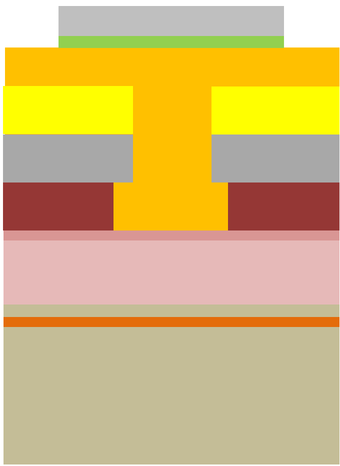


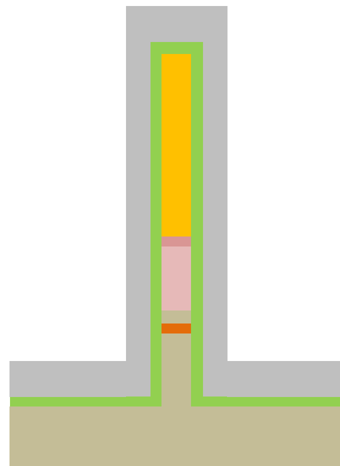


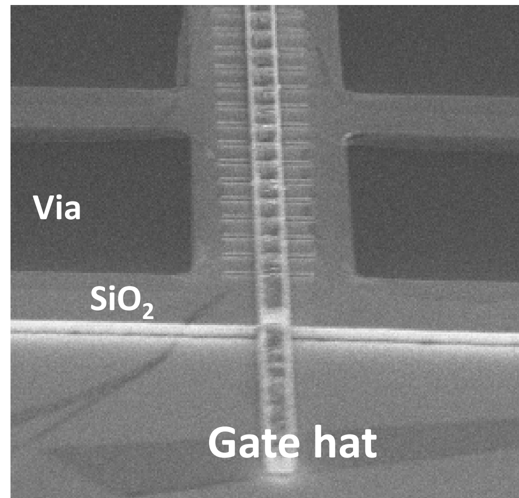


- Double gate FinFET
- Al_2O_3/HfO_2 , EOT = 1 nm

Device fabrication



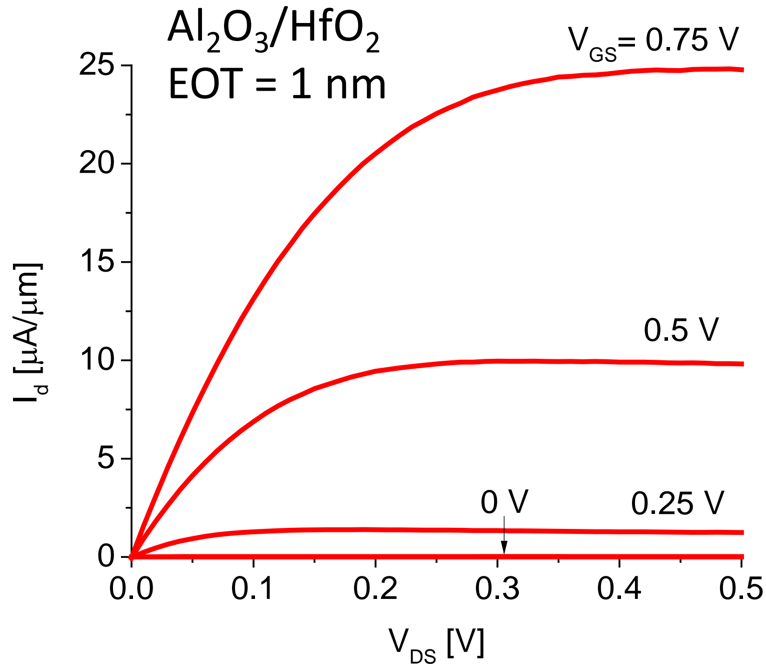


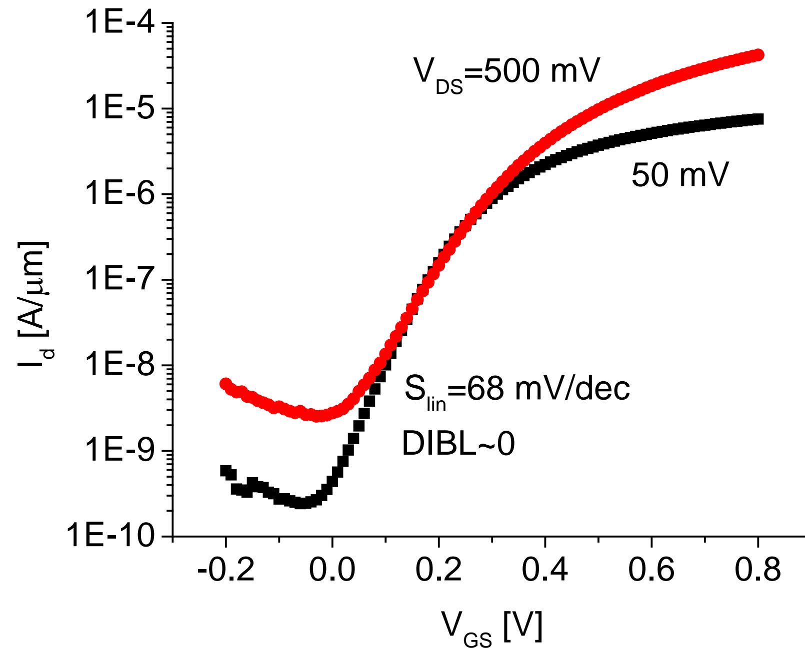


- Fin pitch 200 nm
- 10-50 fins/device

- Sputtered W/Mo contact
- CVD SiO_2 hard mask
- Gate lithography
- Gate recess (Dry): SiO_2/W/Mo
- Active area definition
- Gate recess (Wet): Cap etch
- Fin Lithography
- Fin etch
- Digital etching
- ALD gate dielectric deposition
- Mo gate sputtering
- Gate head photo and pattern
- ILD1 deposition
- Via opening
- Pad formation

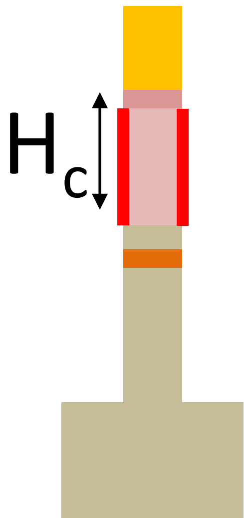
Long channel characteristics, W_f=22 nm, L_g=2 μm

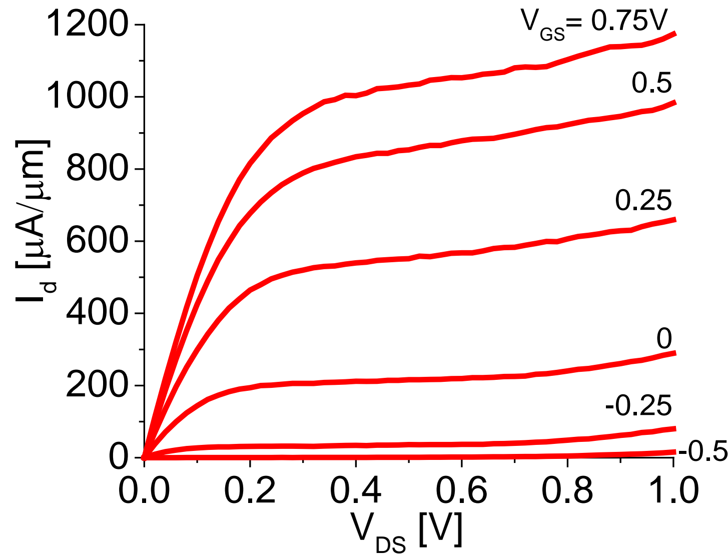


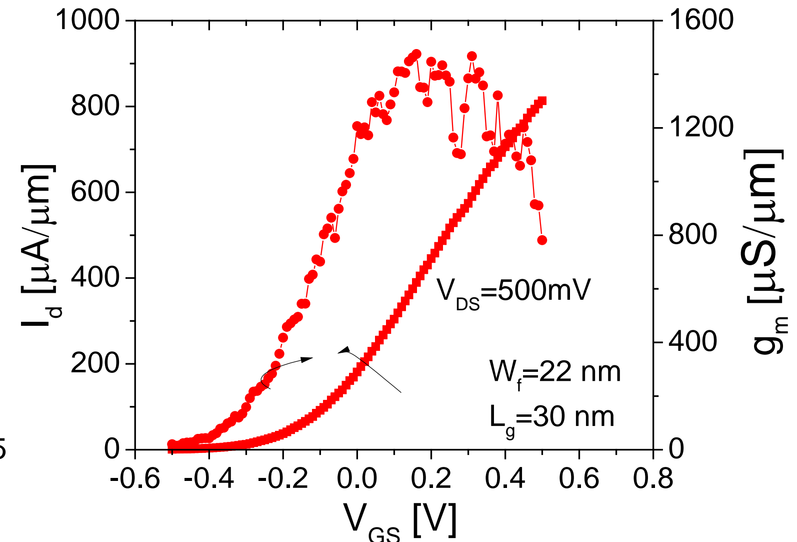


- S_{lin}=68 mV/dec
- Negligible DIBL
- Good electrostatic control over dry etched sidewalls

Short channel characteristics, W_f=22 nm, L_g=30 nm

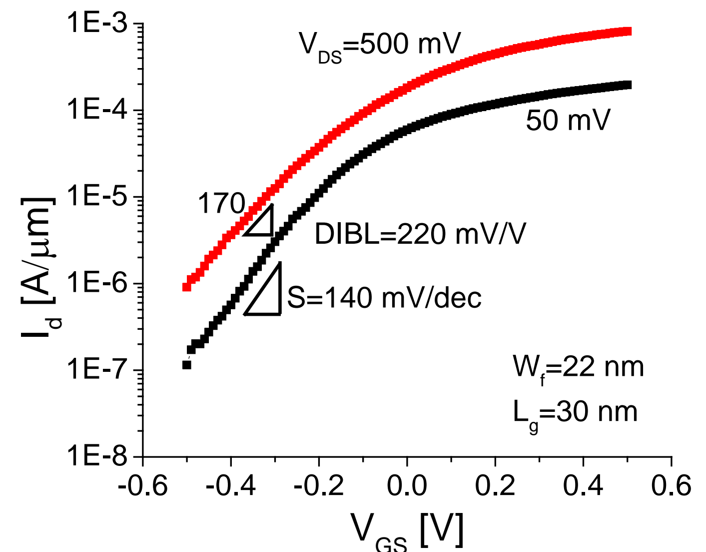




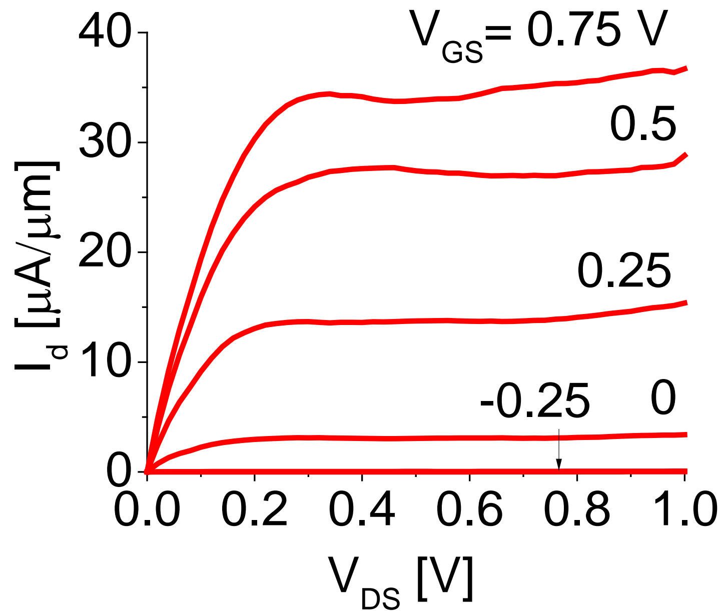


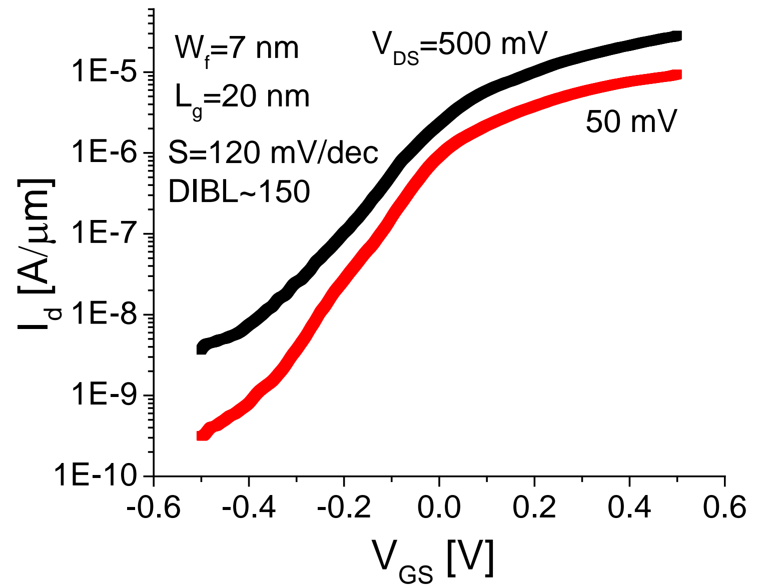
Current normalized by $2 \mathrm{x} H_c$

- AR_c~2
- $g_{m,max}$ = 1.4 mS/µm at V_{DS}=0.5 V
- R_{on}=170 Ω·µm



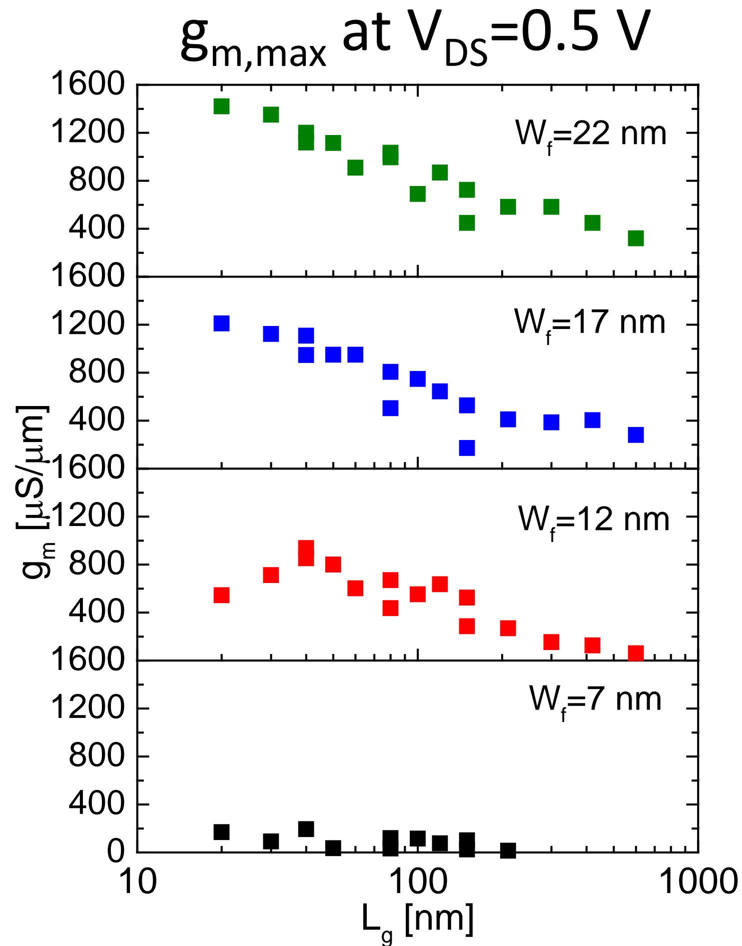
Most aggressively scaled device, W_f=7 nm, L_g=20 nm





- AR_c~6
- Poor drive current → Increased line edge roughness for W_f<10 nm

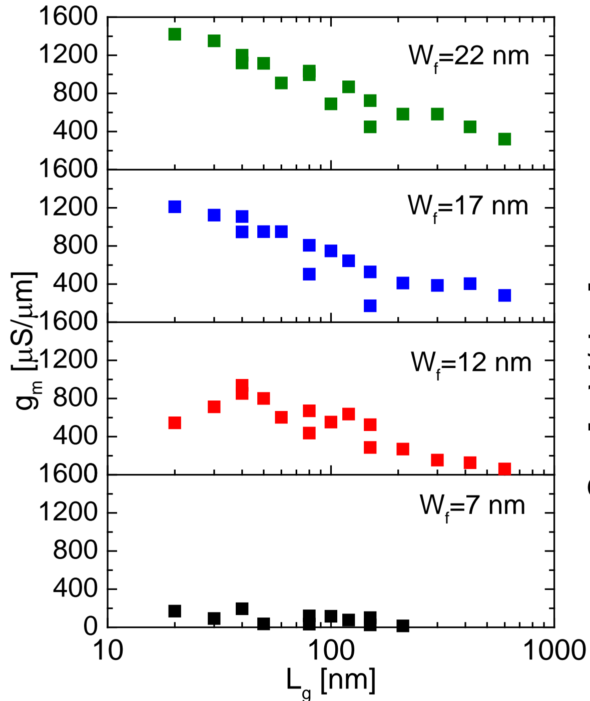
L_g and W_f scaling



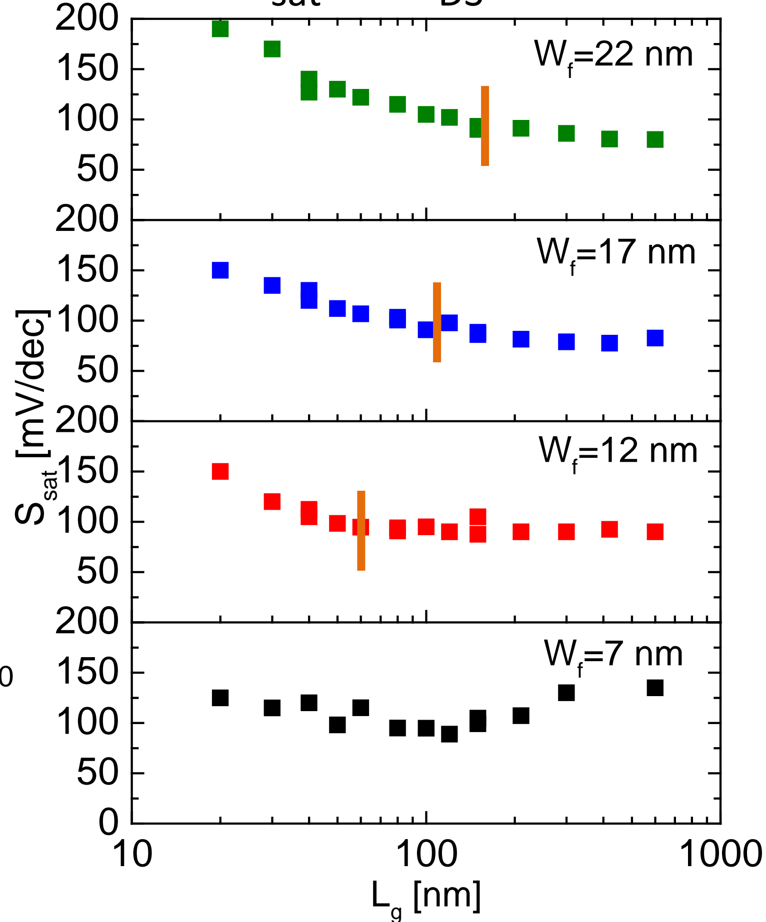
- $L_g \downarrow \rightarrow g_m \uparrow$
- $W_f \downarrow \rightarrow g_m \downarrow$

L_g and W_f scaling

$g_{m,max}$ at V_{DS}=0.5 V



S_{sat} at V_{DS}=0.5 V

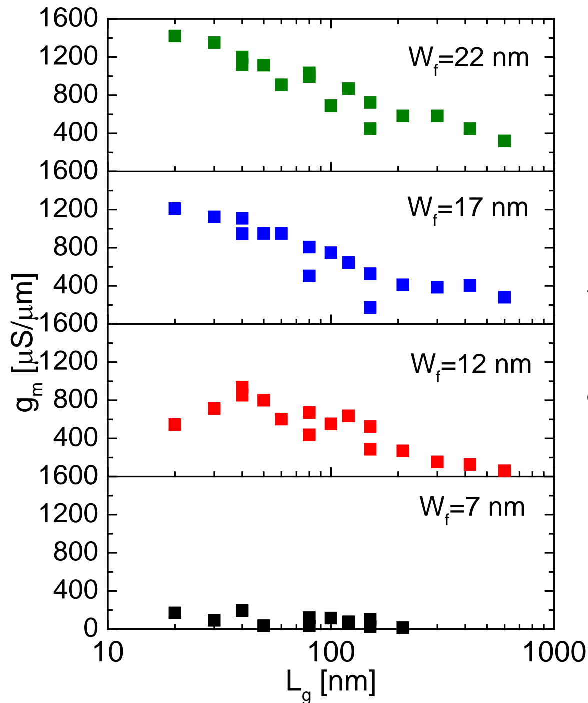


- $L_g \downarrow \rightarrow g_m \uparrow$
- $W_f \downarrow \rightarrow g_m \downarrow$

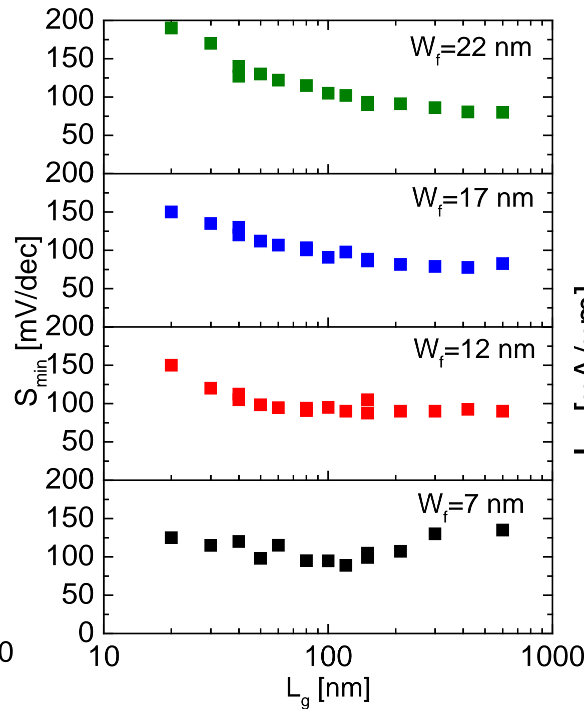
- $W_f \downarrow \rightarrow L_g$ @ onset of SCE$\downarrow$

L_g and W_f scaling

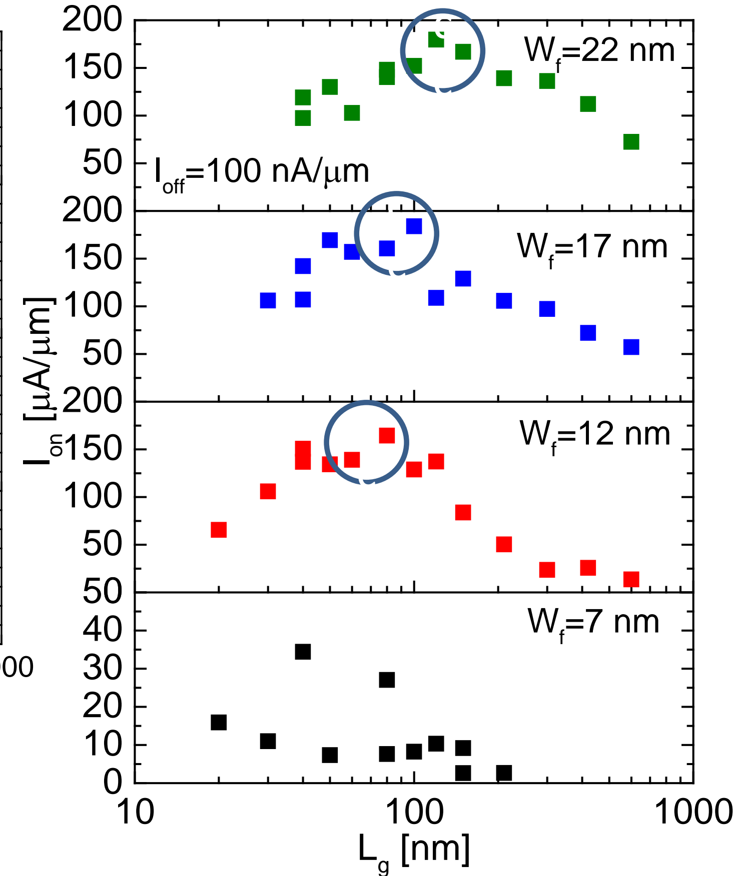
$g_{m,max}$ at v_{DS}=0.5 V



S_{sat} at V_{DS}=0.5 V



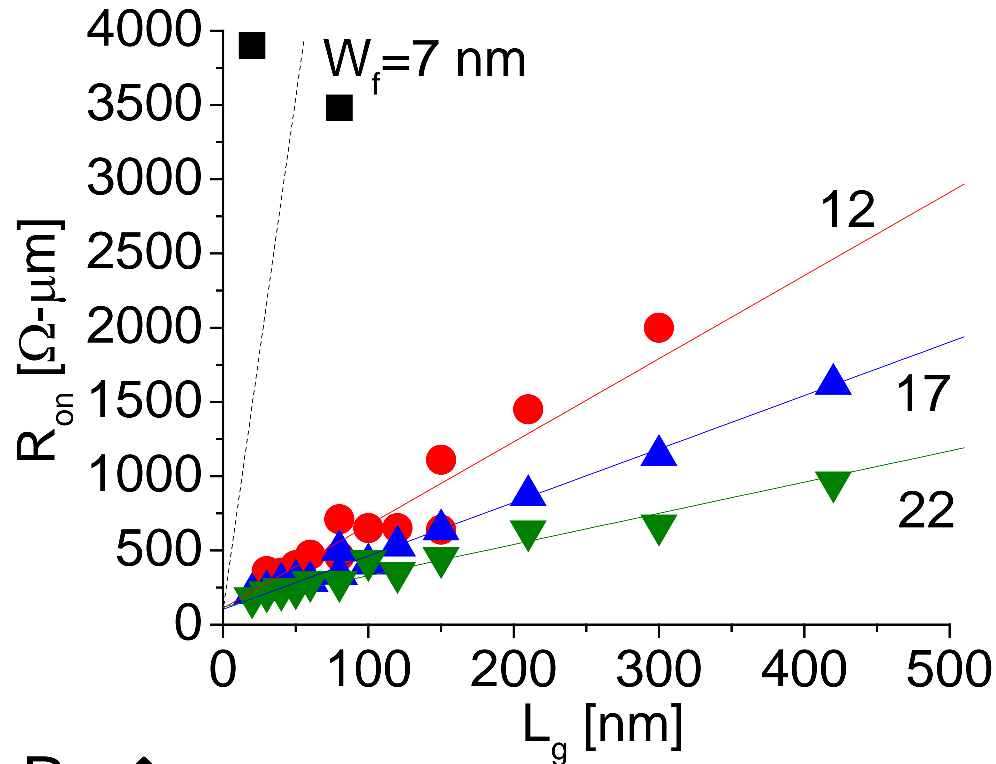
I_{on} at I_{off}=100 nA/μm



- $L_g \downarrow \rightarrow g_m \uparrow$
- $W_f \downarrow \rightarrow g_m \downarrow$
- $W_f \downarrow \rightarrow L_g$ @ onset of SCE $\downarrow$

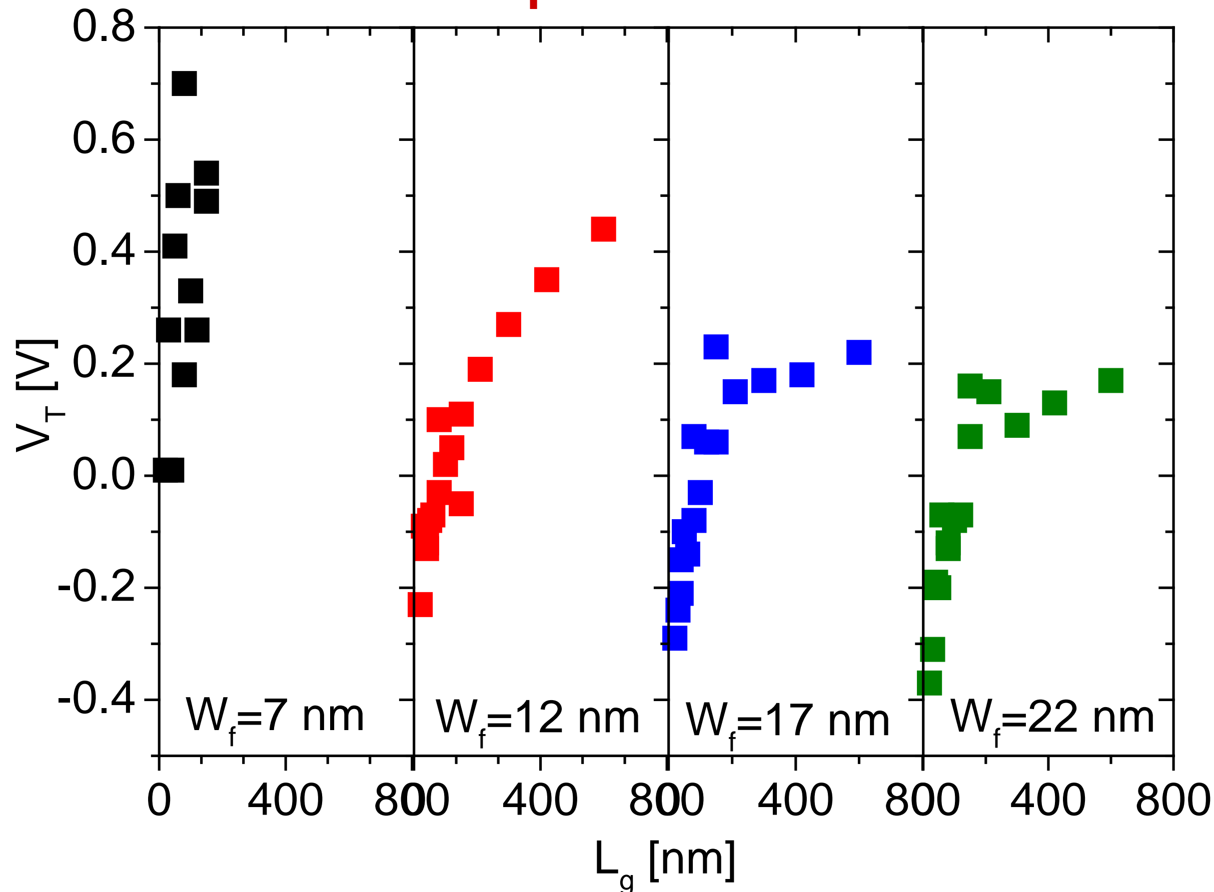
- $W_f \downarrow \rightarrow L_g$ @ max $I_{on} \downarrow$

ON resistance scaling



- $W_f \downarrow \rightarrow R_{on} \uparrow$
- For all W_f , R_{sd}=100 Ω·μm
- Extremely low series resistance due to contact first and self-aligned approach

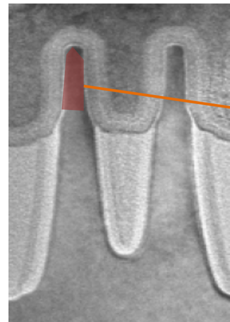
V_T rolloff

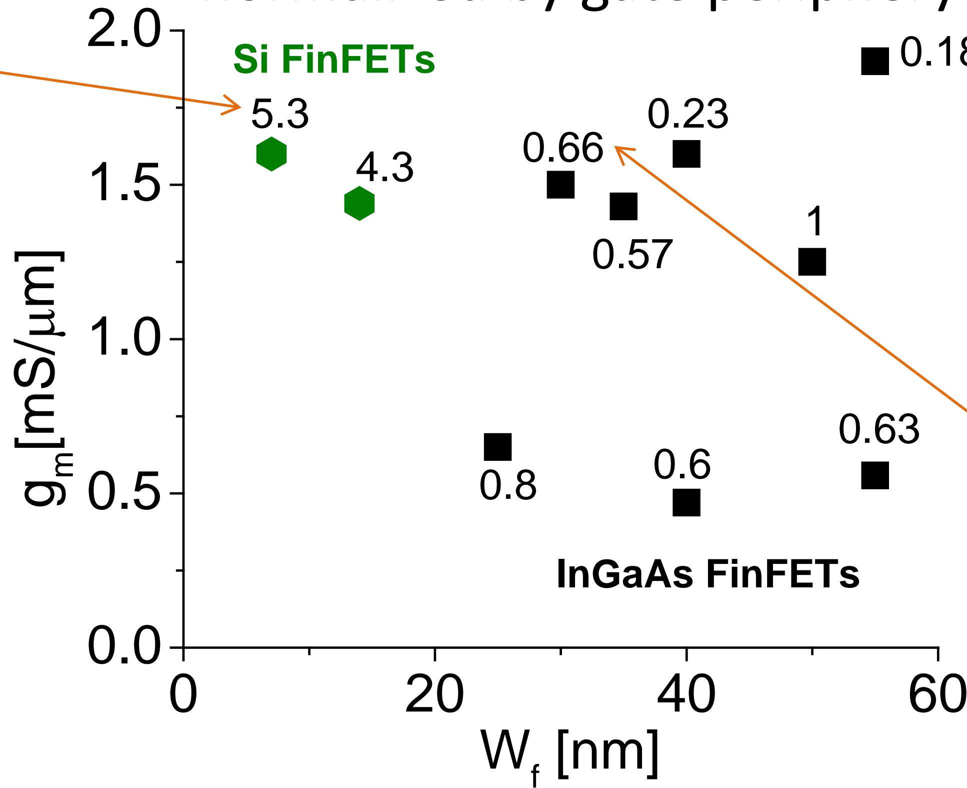


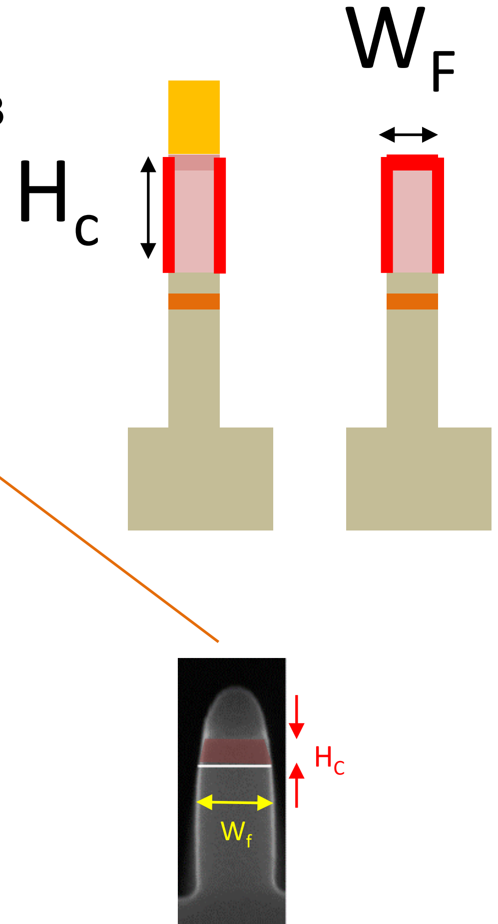
- $W_f \downarrow \rightarrow V_T \uparrow \rightarrow$ delta doping, quantization
- $W_f \downarrow \rightarrow V_T$ rolloff $\uparrow \rightarrow$ line edge roughness ?

A. Vardi, IEDM 2015

Benchmark

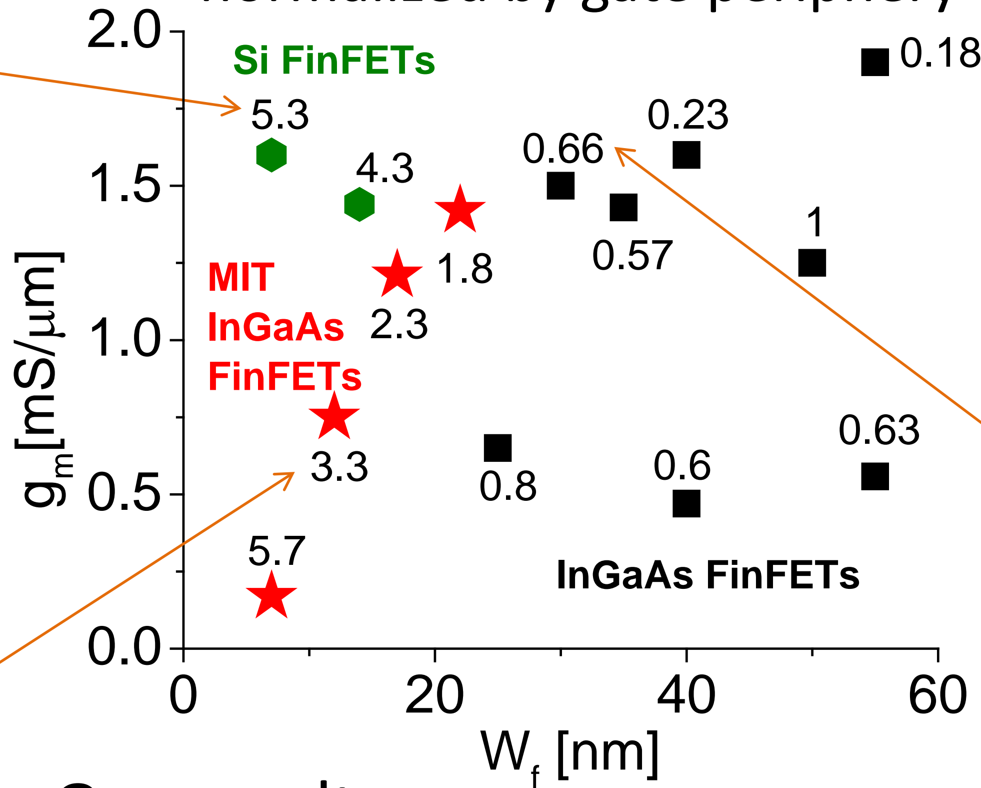


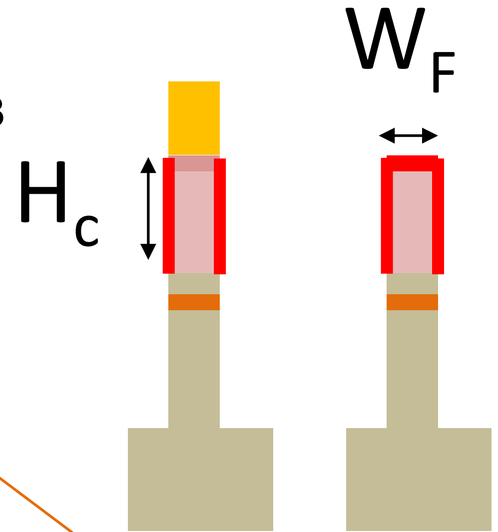


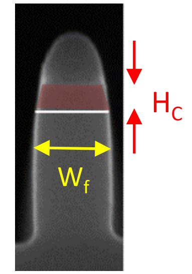


- g_m of Si ~ g_m of III-V
- III-V FinFET $AR_c \leq 1$

Benchmark





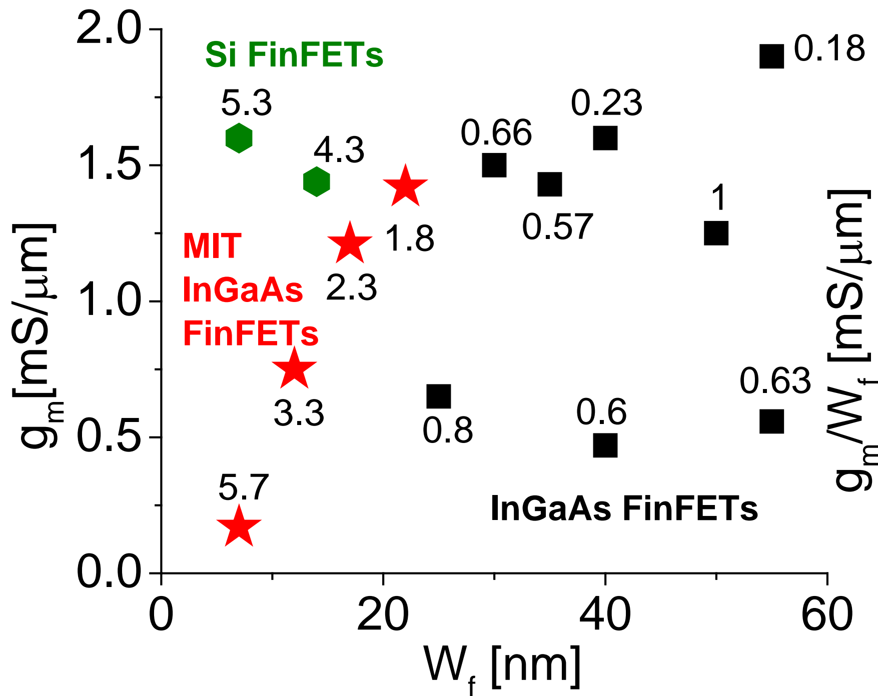


Our results:

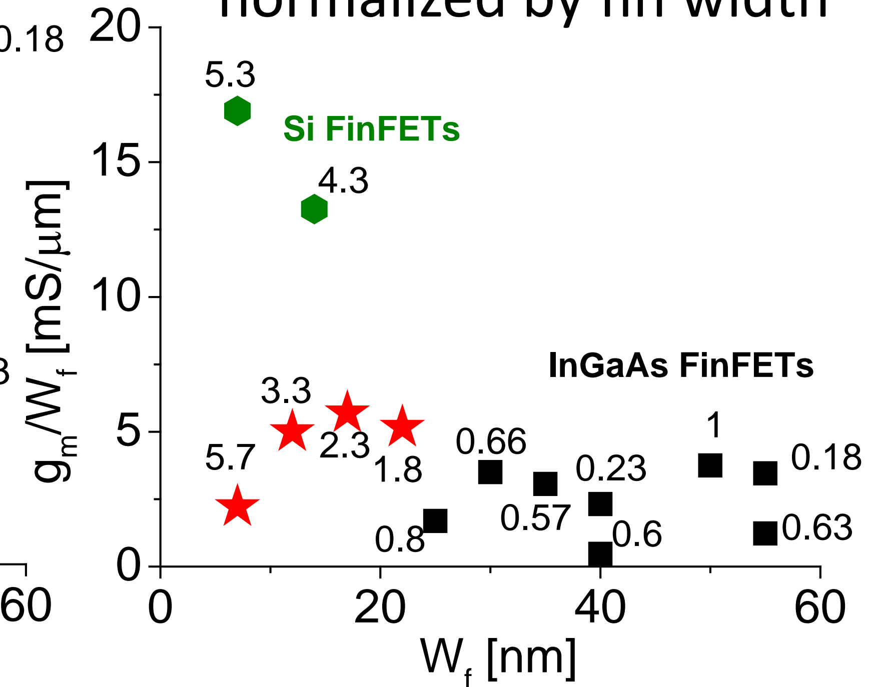
- AR_c>1 for the first time in III-V
- Sub-20 nm W_f
- W_f ↓ → g_m ↓

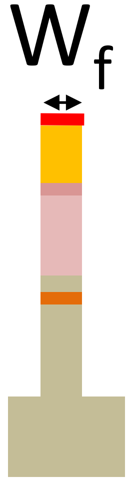
Benchmark

Physical g_m:



Footprint g_m:
normalized by fin width



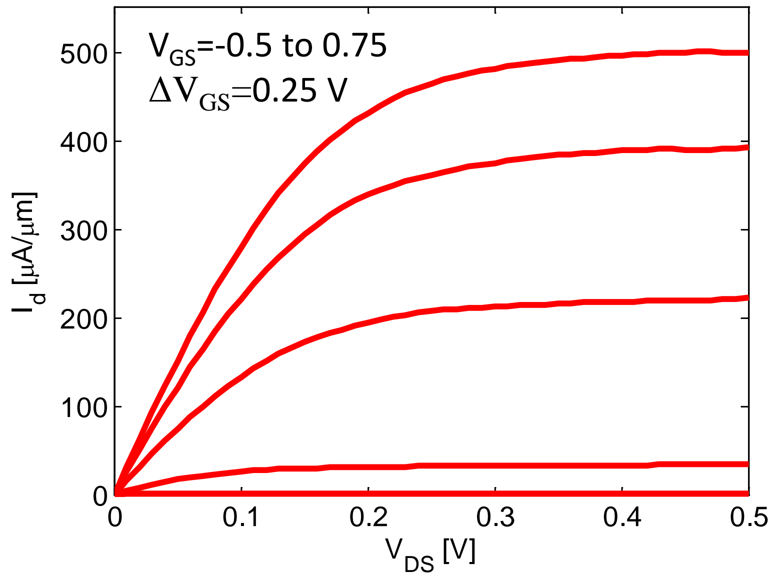


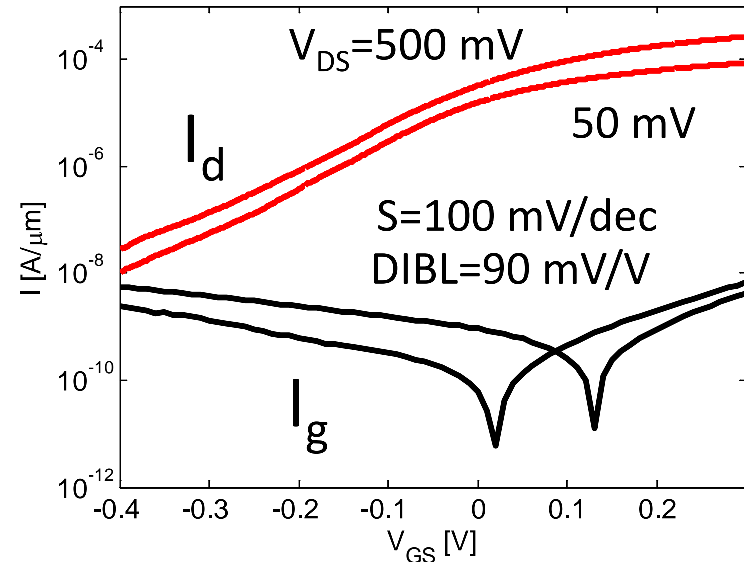
For g_m/W_f:

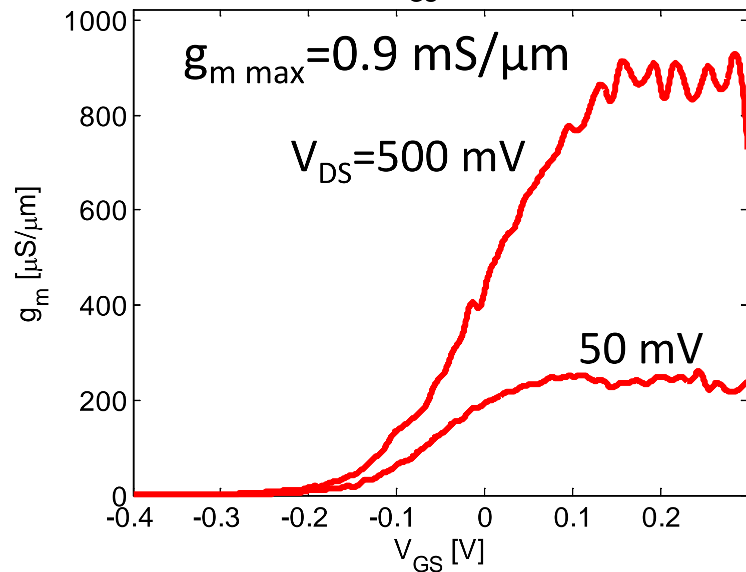
- Si >> III-V
- MIT FinFETs > all other III-V
  - → good use of sidewall conductance

→ Our results improve the state-of-art

Post-submission results



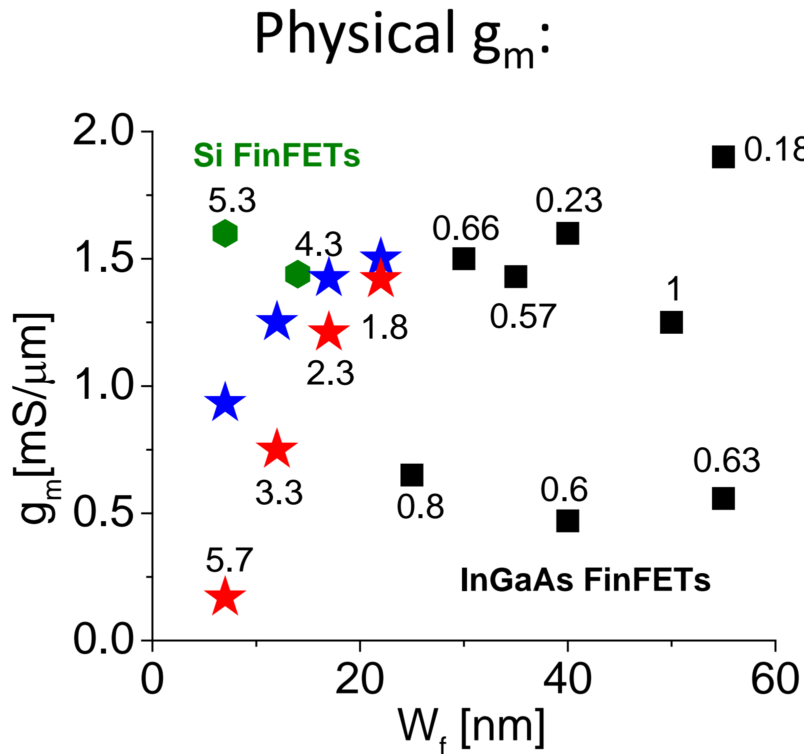




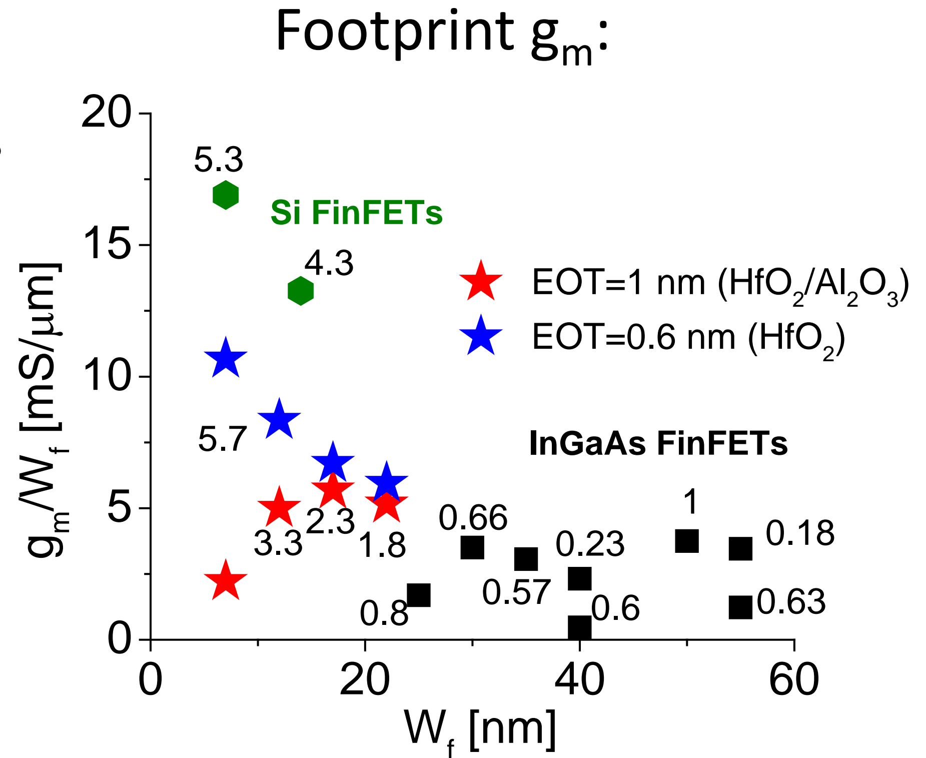
W_f=7 nm
L_g=30 nm
EOT=0.6 nm (HfO_2)

Benchmark with latest results

Physical g_m:



Footprint g_m:



- New record results for sub-10 nm W_f InGaAs FinFETs

Conclusions

- Novel self-aligned gate-last FinFET:
  - Self-aligned gate to contact metals
  - CMOS process compatibility
  - Sub-10 nm fin width
  - AR_c>1 for the first time in III-V
  - Double-gate FinFET
- Outstanding performance and short-channel effects in devices with L_g=30 nm and W_f=22 nm
- Demonstrated subthreshold swing of 68 mV/dec in long channel devices

Thank you !